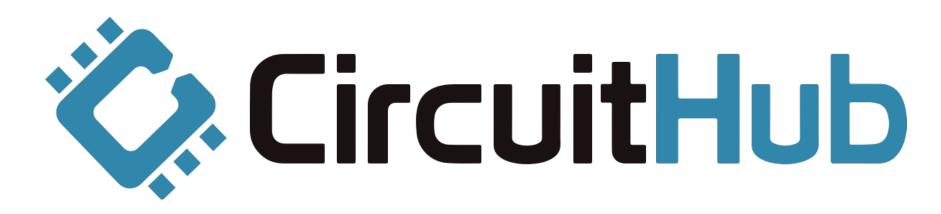


Your Manufacturer Is Stupid

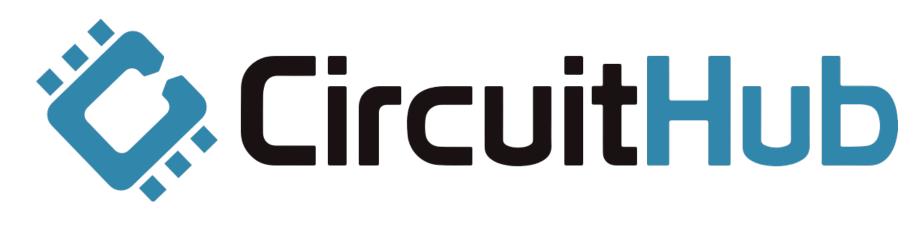
Help Them

Chris Denney

CTO - Worthington Assembly



Chris Denney



Chris Denney

Jerk Who Tells You There's A Problem



Your Manufacturer Is Stupid

Have to act stupid



Your Manufacturer Is Stupid

Play dumb on new products



The Problem



Information about your design is unclear

Phone calls needs to be made



The Problem



I hate people calling me. I hate calling people.





The Problem



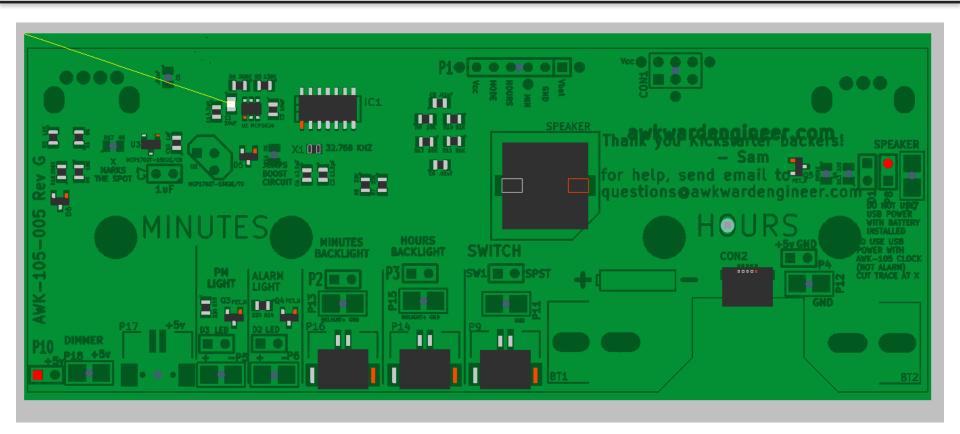
But machines build things!





Actually, humans build things

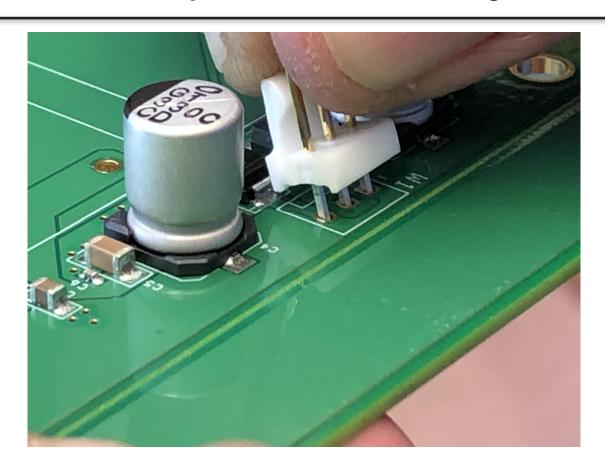






Actually, humans build things

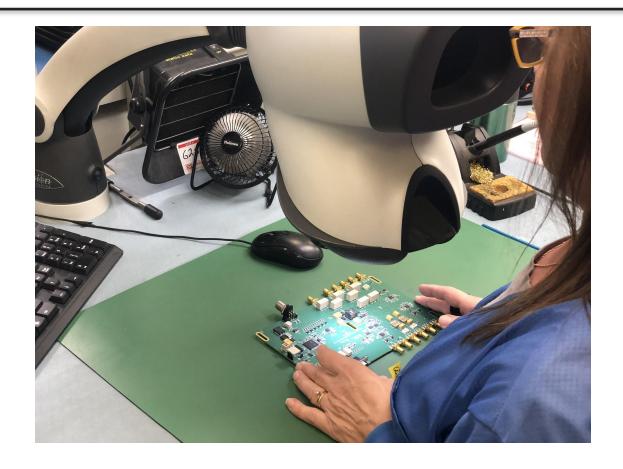






Actually, humans build things











- 1. Identifying polarity of components
- 2. Silkscreen legibility
- 3.Panelization
- 4.PCB properties
- 5. Specific manufacturer's part numbers





- 1. Identifying polarity of components
- 2. Silkscreen legibility
- 3. Panelization
- 4.PCB properties
- 5. Specific manufacturer's part numbers







The number 1 problem



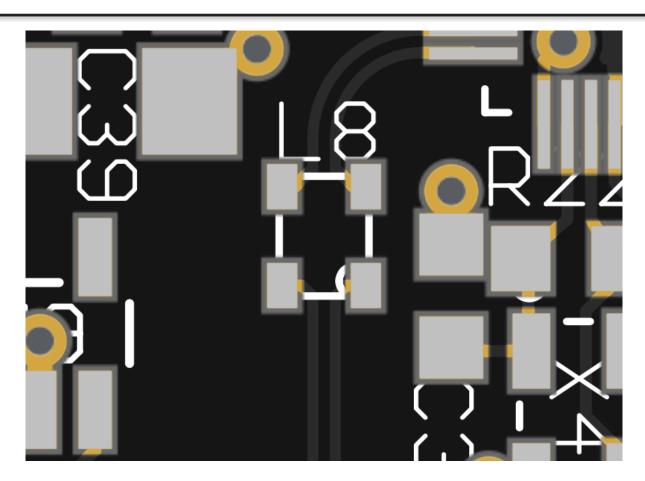
The Assembly Made for the First Time



- Polarity of all IC's
 - What is this IC's reference designator?
 - Which pad is Pin 1
- Polarity of all diodes
- Polarity of all LED's
 - This LED here, what reference designator is it?
 - Which pad is the cathode?

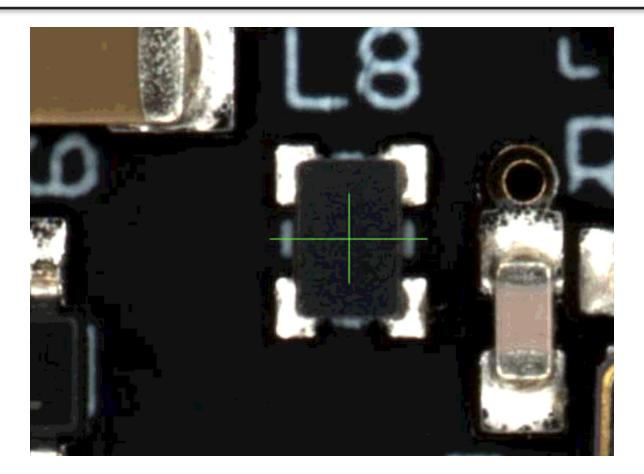






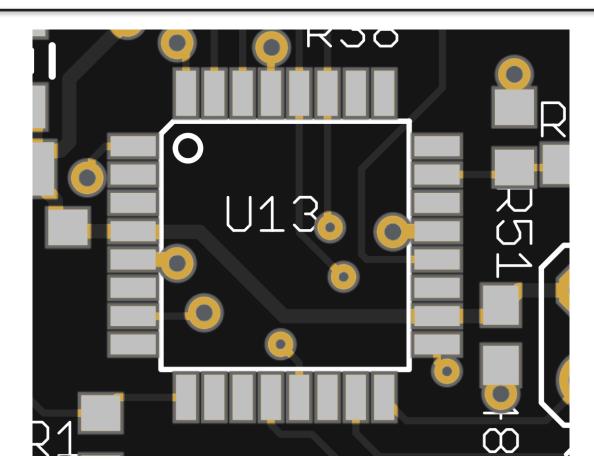






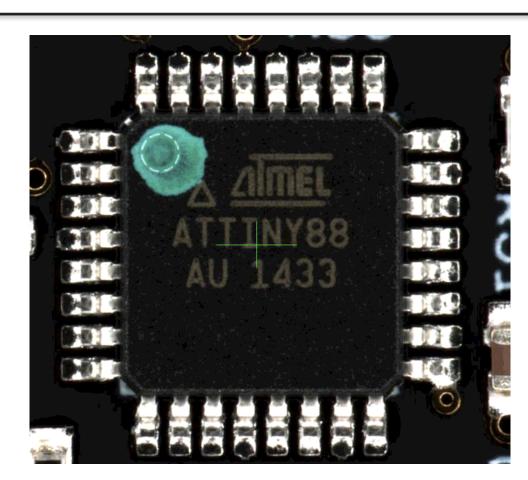






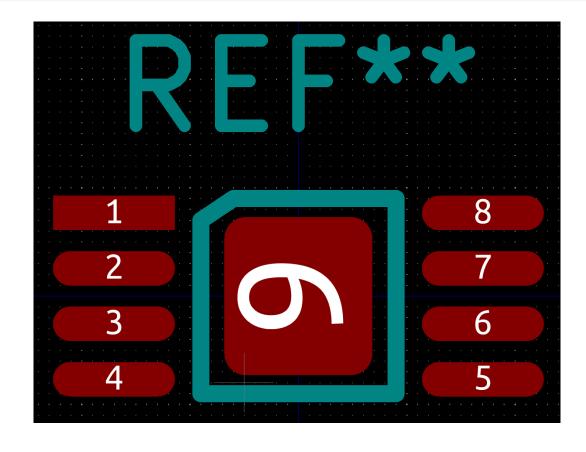






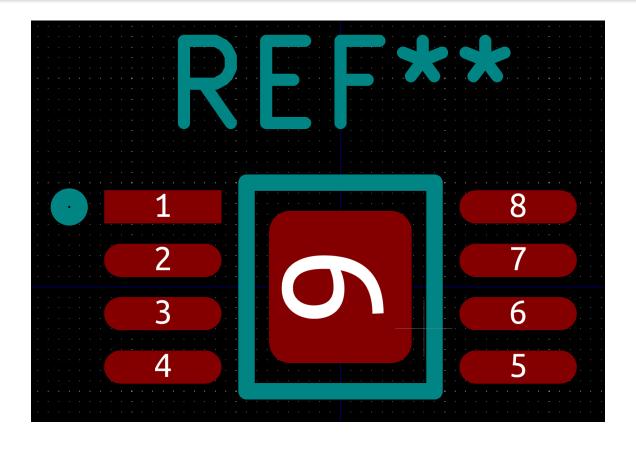






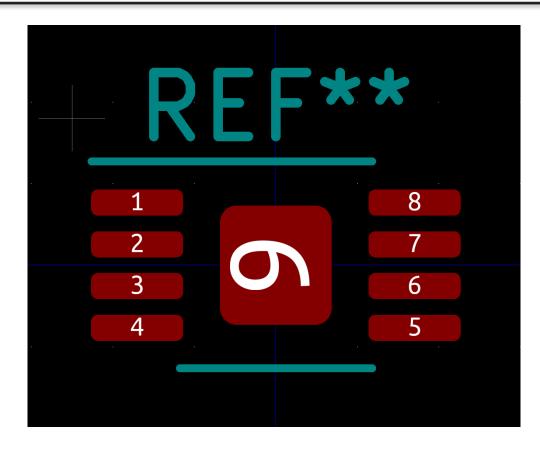






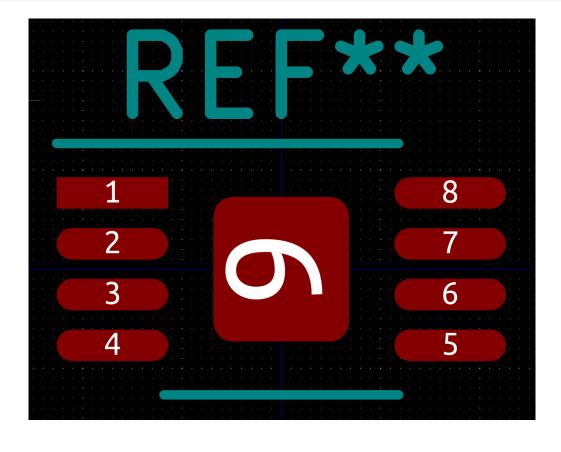






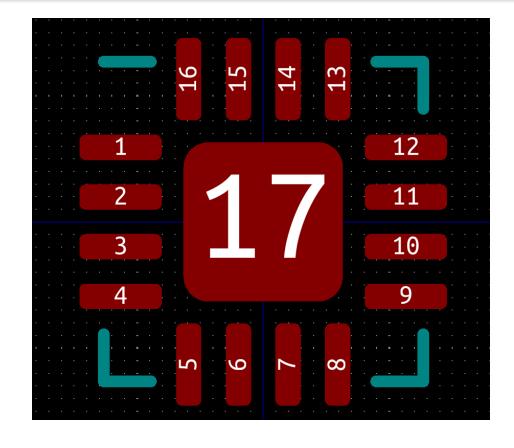






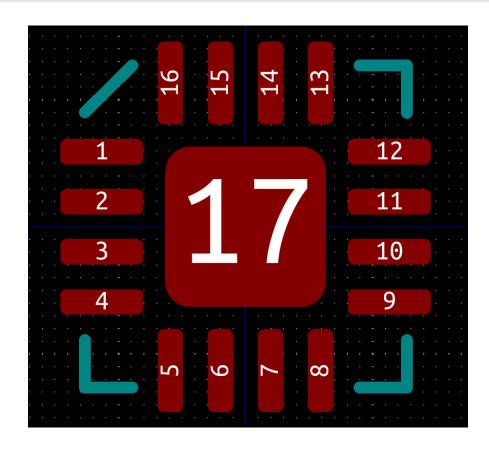






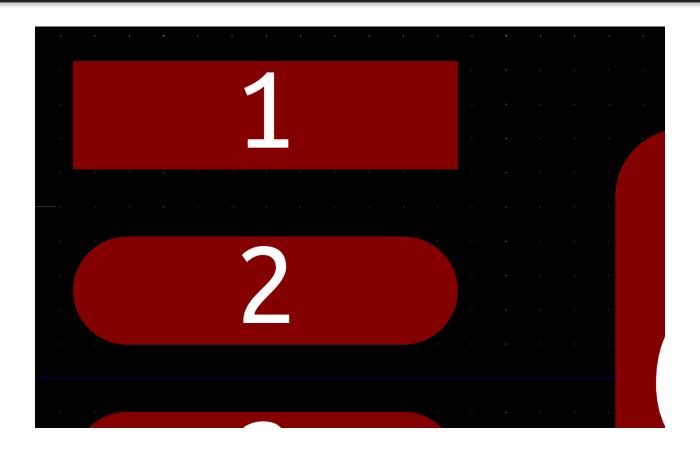
















				Pad Propertie	S	
Gen	eral Local Clearance and S	ettings	Custom Shar	pe Primitives		Footprint REF** (LFCSP-16-1EP_3x3mm_P0.5mm_EP1.6x1.6mm)
Pad number:	1		Hole shape:	Circular	\$	front side, rotated 0.0 deg
Net name:	<no net=""></no>	~	Hole size X:	0	mm	
Pad type:	SMD		Hole size Y:	0	mm	
Shape:	Rounded Rectangle		Common	F.O.,	•	
Positi . A:	-1.4375	mm	Copper:			
Position Y:	-0.75	mm	Technical layers: F.Adhes B.Adhes F.Paste B.Paste F.SilkS			
Size X:	0.825	mm				1
Size Y:	0.25	mm				
Orientation:	0.0	deg				
Shape offset X:	0	mm	B.SilkS			
Shape offset Y:	0	mm	✓ F.Mask			
Pad to die length:	0	mm	B.Mask Dwgs.User Eco1.User			
Trapezoid delta:	0	mm				
Trapezoid axis:	Vertical	\$	Eco2.U	Iser		-
Corner size:	25.0	%				Show pad in outline mode
	0.0625	mm				





0		Pad Properties	S
Gen	eral Local Clearance and Settings	Custom Shape Primitives	Footprint REF** (LFCSP-16-1EP_3x3mm_P0.5mm_EP1.6x1.6mm),
Pad number: Net name:	Circular Oval	Hole shape: Circular Hole size X: 0	front side, rotated 0.0 deg
Pad type:	Rectangular Trapezoidal / Rounded Rectangle	Hole size Y: 0 Copper: F.Cu	mm
Position X: Position Y:	Custom (Circ. Anchor) Custom (Rect. Anchor) -0.75 mm	Technical layers:	
Size X: Size Y:	0.825 mm 0.25 mm	B.Adhes F.Paste	
Orientation: Shape offset X:	0.0 deg	B.Paste F.SilkS B.SilkS	
Shape offset Y: Pad to die length:	0 mm	✓ F.Mask ■ B.Mask	
Trapezoid delta:	0 mm	Dwgs.User Eco1.User Eco2.User	
Trapezoid axis: Corner size:	Vertical \$ 25.0 %	2002.0361	Show pad in outline mode
Corner radius:	0.0625 mm		Cancel

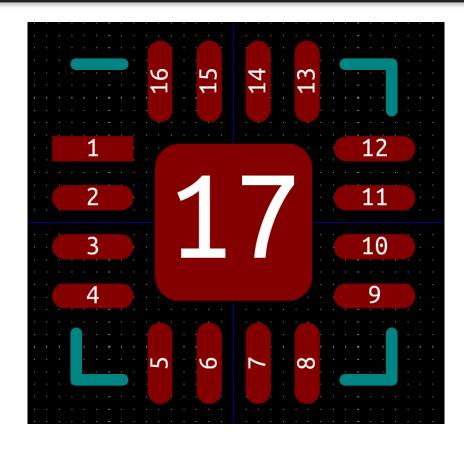




Gen	eral Local Clearance and Se	ettings	Custom Shape Primitives		Footprint REF** (LFCSP-16-1EP_3x3mm_P0.5mm_EP1.6x1.6mm)
Pad number:	Circular		Hole shape: Circular	\$	front side, rotated 0.0 deg
Net name:	Oval		Hole size X: 0	mm	
Pach , pe:	Rectangular Trapezoidal		Hole size Y: 0	mm	
Shape:	Rounded Rectangle		Copper: F.Cu		
Position X:	Custom (Circ. Anchor) Custom (Rect. Anchor)	mm	Technical layers:	~	
Position Y:	-0.25	mm	F.Adhes		
Size X:	0.825	mm	B.Adhes		2
Size Y:	0.25	mm	✓ F.Paste		
Orientation:	0.0	deg	B.Paste F.SilkS		
Shape offset X:	0	mm	B.SilkS		
Shape offset Y:	0	mm	✓ F.Mask ■ B.Mask ■ Dwgs.User ■ Eco1.User		
Pad to die length:	0	mm			
Trapezoid delta:	0	mm			
Trapezoid axis:	Vertical		Eco2.User		-
Corner size:	25.0	%			Show pad in outline mode
Corner radius:	0.0625	mm			

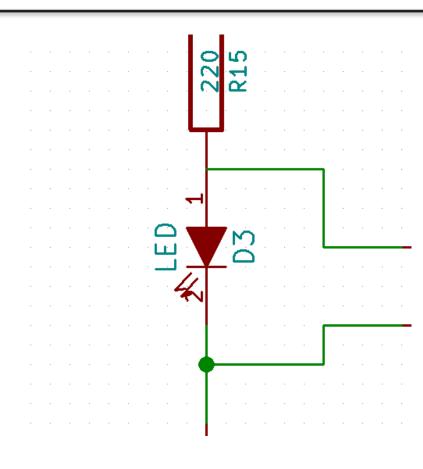






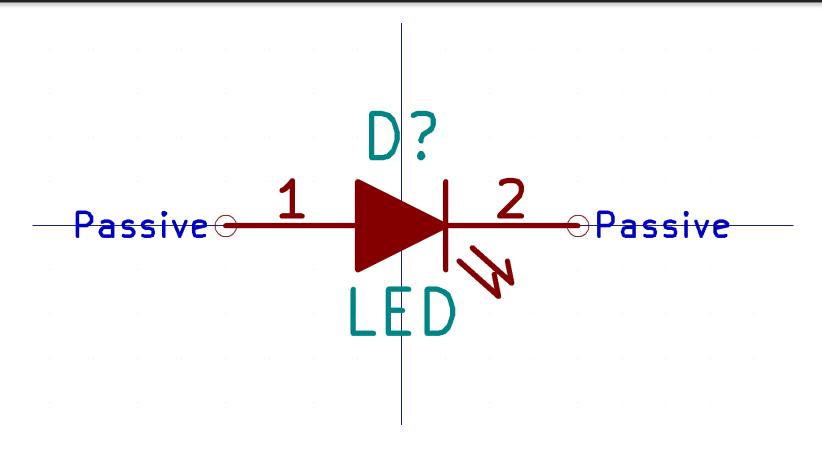






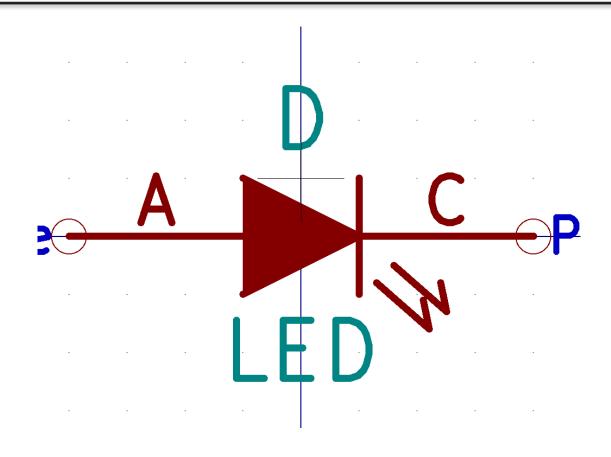












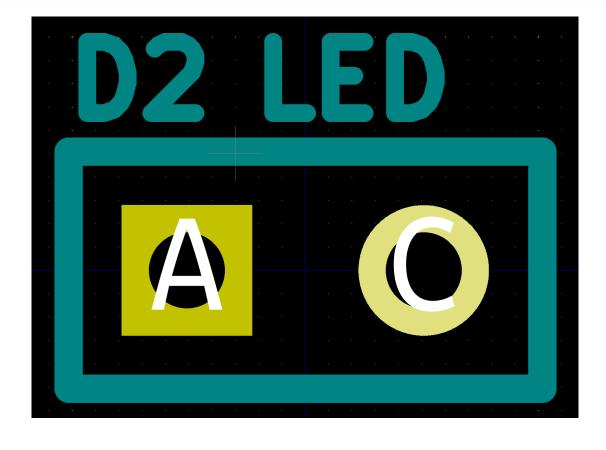




		Pin Prop	perties
Pin name: Pin number: Electrical type: Graphic style: X position: Y position: Orientation: Pin length: Name text size: Number text size:	C C H Passive Line 5.080 0.000 Left 3.810 1.016	mm mm mm mm	□ Common to all units in symbol □ Common to all body styles (DeMorgan) ✓ Visible
			Cancel OK

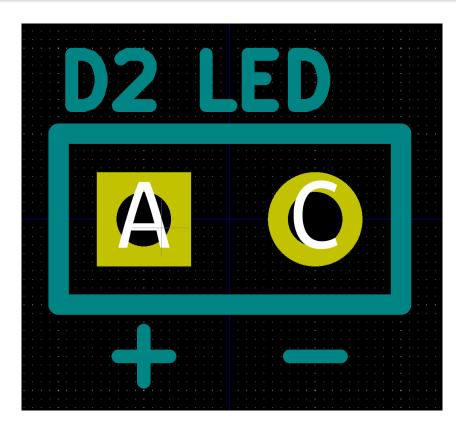






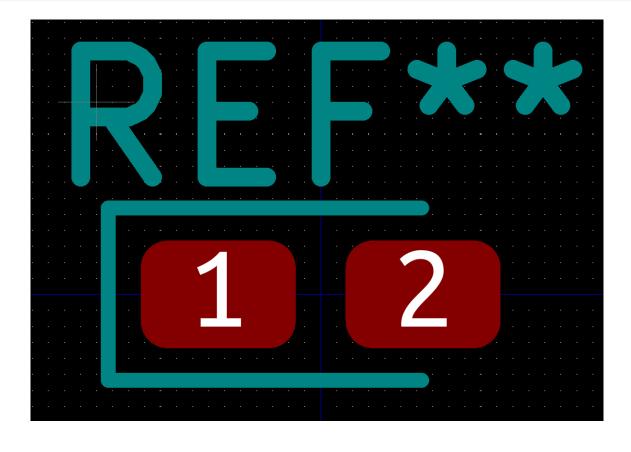






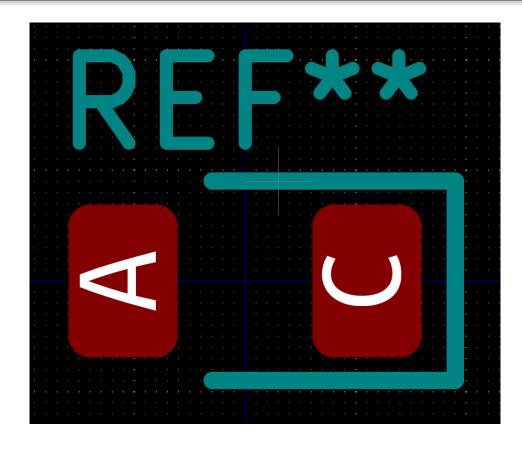






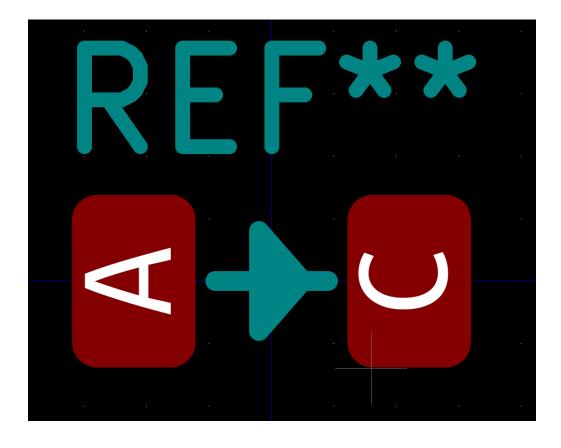






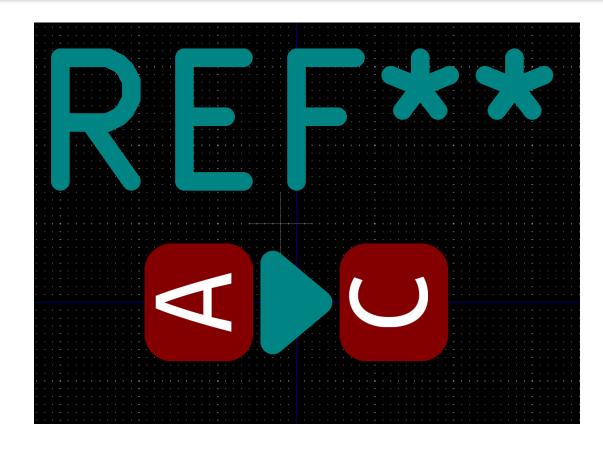














Identifying Polarity - Summary



- 1. Silkscreen pin 1 indicators
 - a. Move them out from underneath the placed part
 - b. Square pad for Pin 1 on IC's
- 2. LED cathode indicators
 - a. Use a C in pin naming scheme
 - b. Use symbol in silkscreen
 - c. Use + and symbols in silkscreen
 - d. Thru-hole: Square pad for Anode. Circle for Cathode

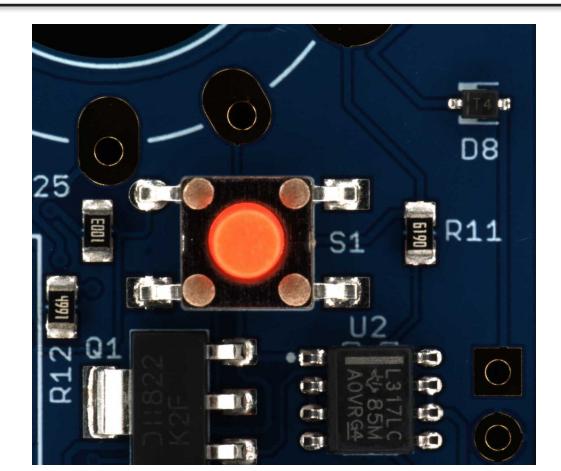




- 1. Identifying polarity of components
- 2. Silkscreen legibility
- 3. Panelization
- 4.PCB properties
- 5. Specific manufacturer's part numbers











Not minimums







Not maximum



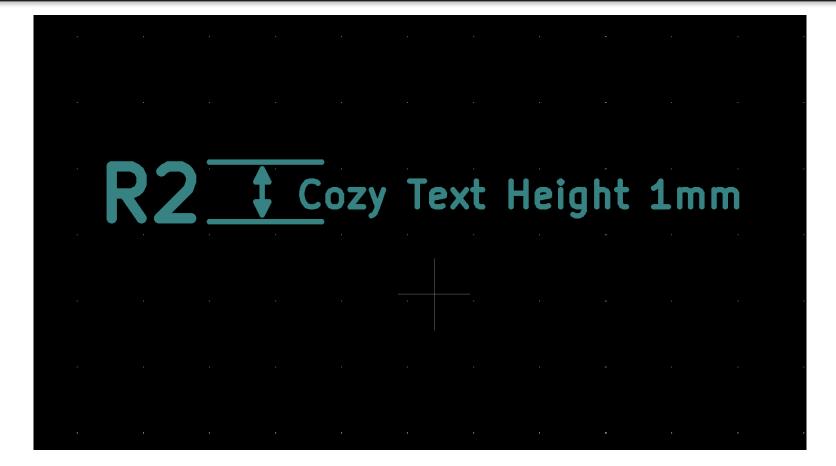


Cozy



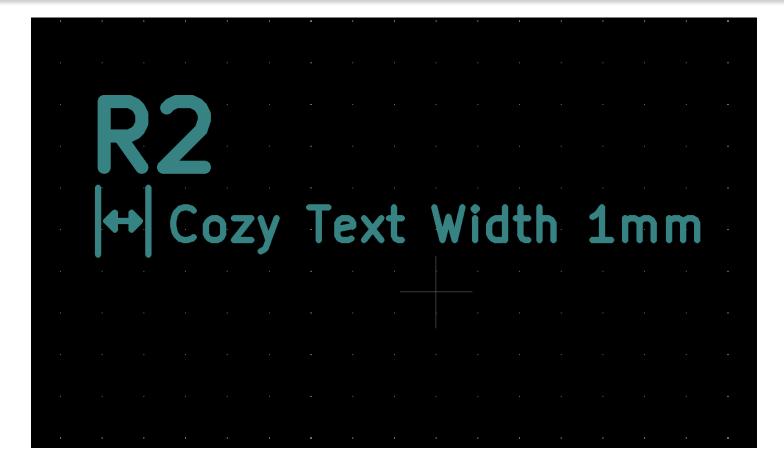






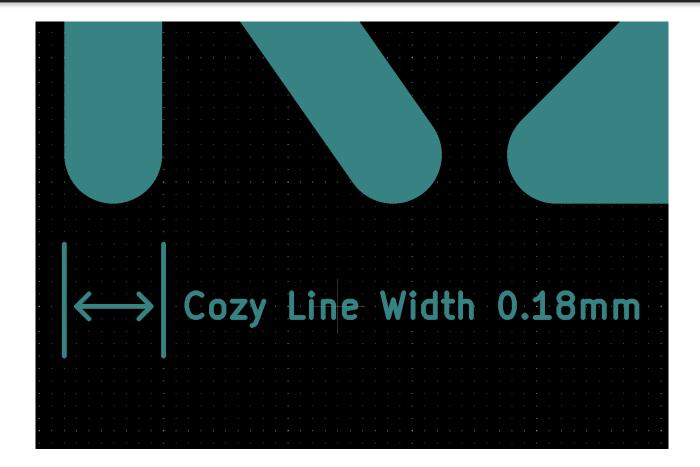






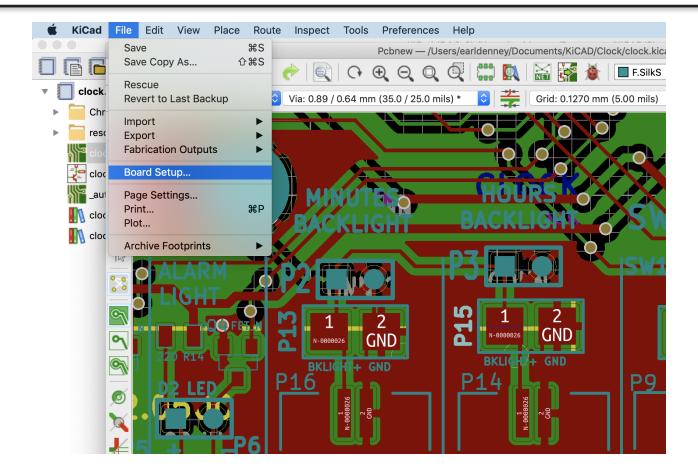






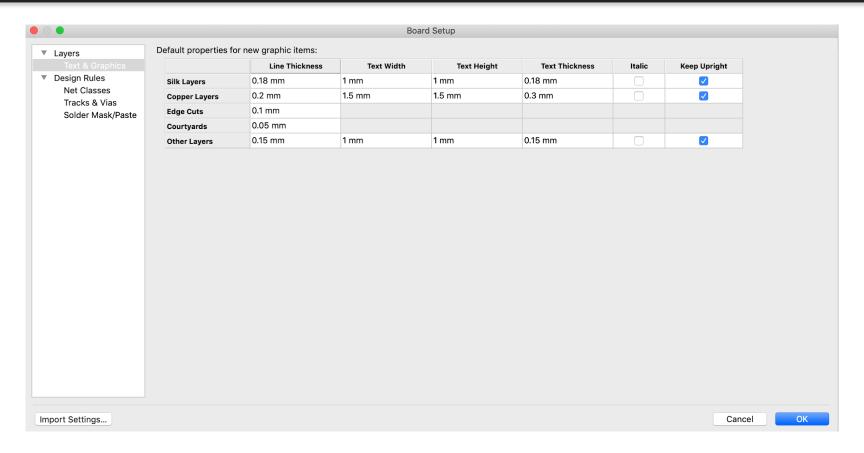












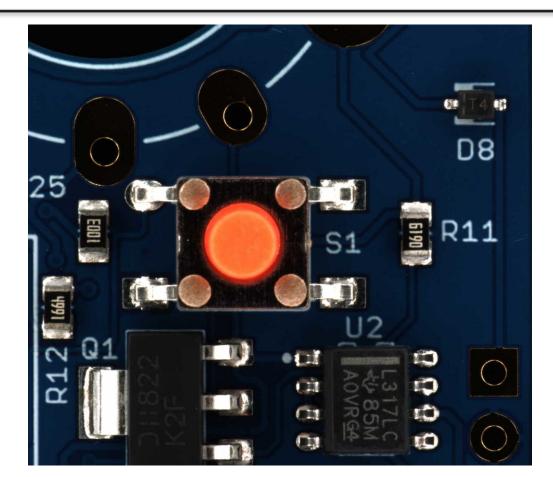




Default properties for new graphic items:								
	Line Thickness	Text Width	Text Height	Text Thickness	Italic	Keep Upright		
Silk Layers	0.18 mm	1 mm	1 mm	0.18 mm		✓		
Copper Lavers	0.2 mm	1.5 mm	1.5 mm	0.3 mm		✓		



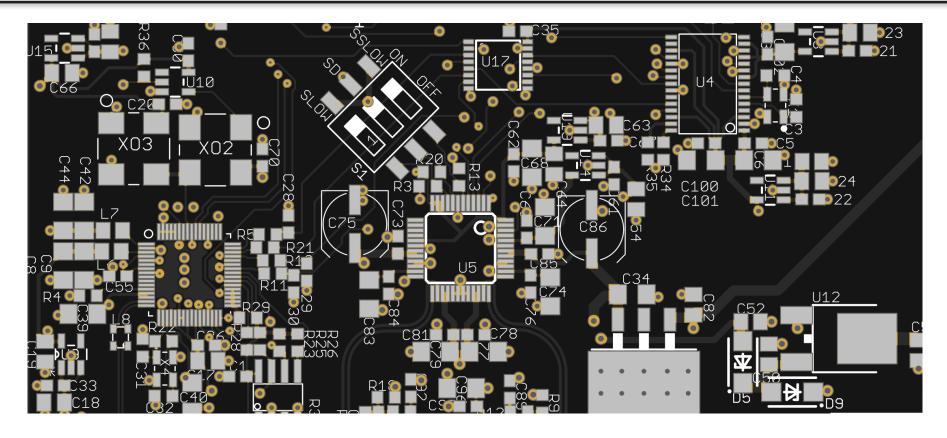






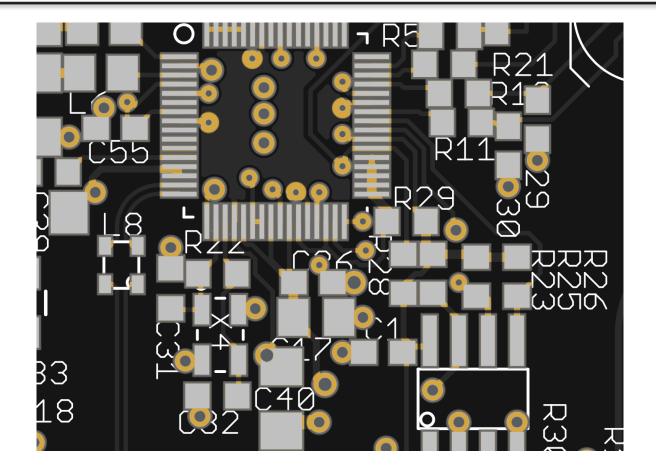
Identifying Polarity





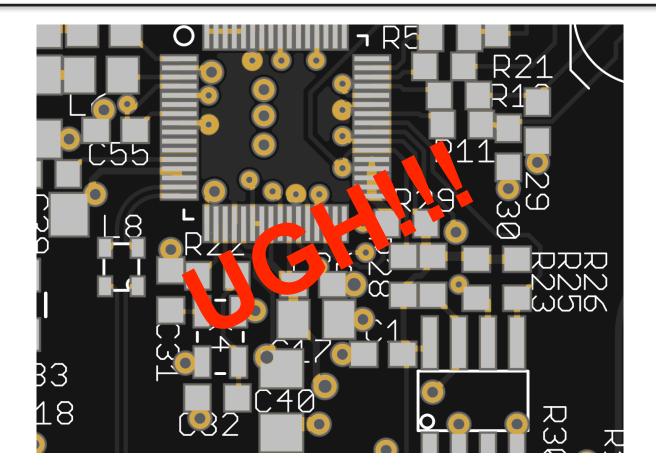






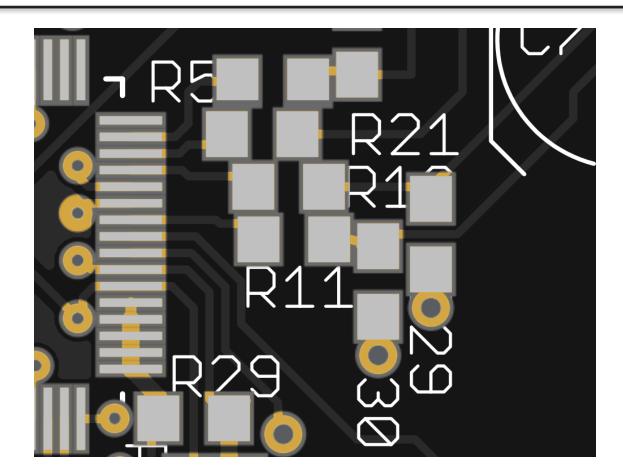






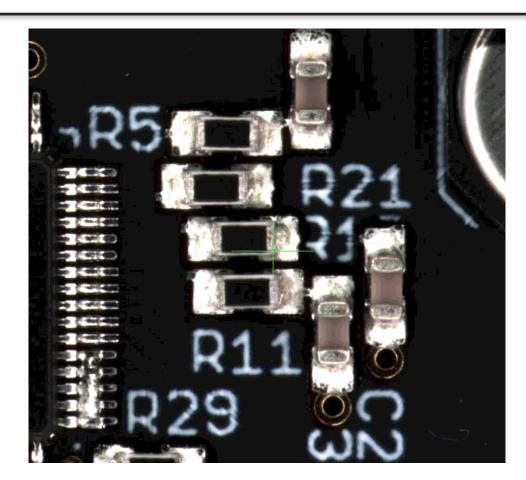












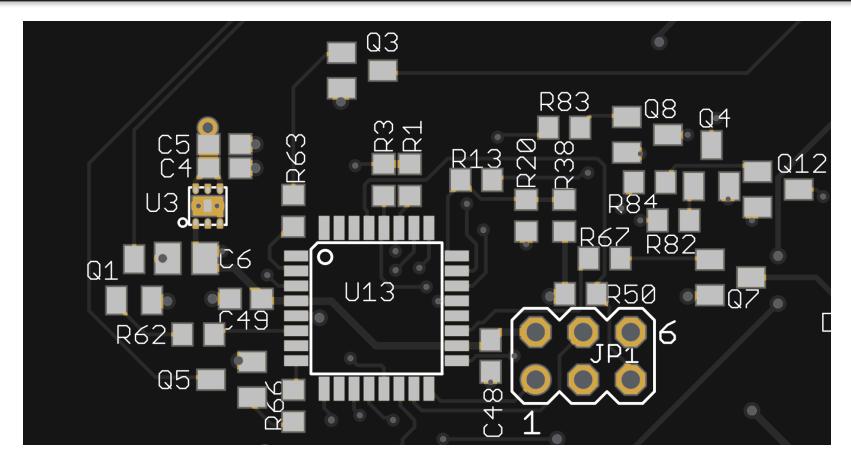




	Plot						
Plot format: Gerber	Output directory: Gerber/						
Included Layers General Options							
F.Cu B.Cu F.Adhes B.Adhes F.Paste B.Paste F.SilkS B.SilkS F.Mask Dwgs.User Cmts.User Fco1.User	Plot border and title block ✓ Plot footprint values ✓ Plot footprint verences ✓ Plot footprint verences Force plot ing of invisible values / refs ✓ Excluse PCB edge layer from other layers ✓ Excluse PCB edge layer from other layers ✓ Excluse PCB edge layer from other layers ✓ By de pads from silkscreen Do not tent vias Use auxiliary axis as origin ✓ Check zone fills before plotting Gerber Options ✓ Use Protel filename extensions Coordinate format: 4.6, unit mm	mm					
Eco2.User Edge.Cuts	Generate Gerber job file ✓ Subtract soldermask from silkscreen Use extended X2 format Include netlist attributes						
Output Messages							
Show: All	ors Varnings Actions Infos						
Run DRC	Close Generate Drill Files Plo	t					

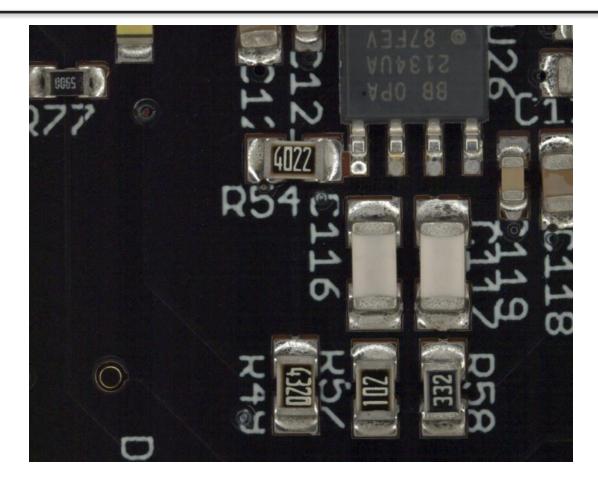




















Silkscreen Legibility - Summary



- 1. Cozy Text: 1x1mm with 0.18mm line width
- 2. Move away from pads, holes, and vias
- 3. Tent vias to print on top of vias but only if you must

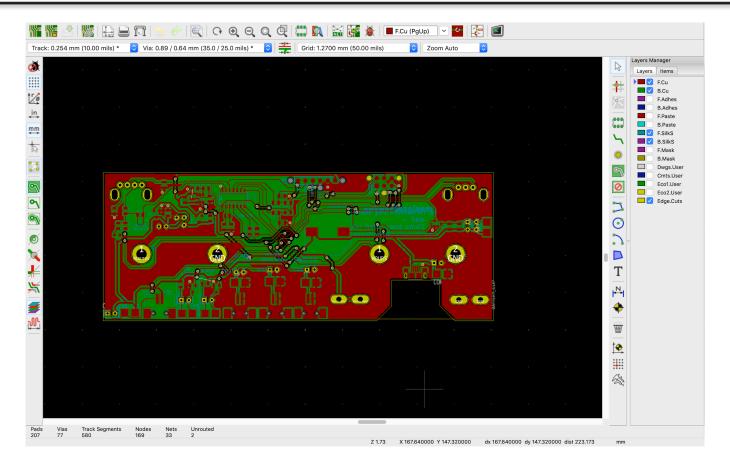




- 1. Identifying polarity of components
- 2. Silkscreen legibility
- 3. Panelization
- 4.PCB properties
- 5. Specific manufacturer's part numbers

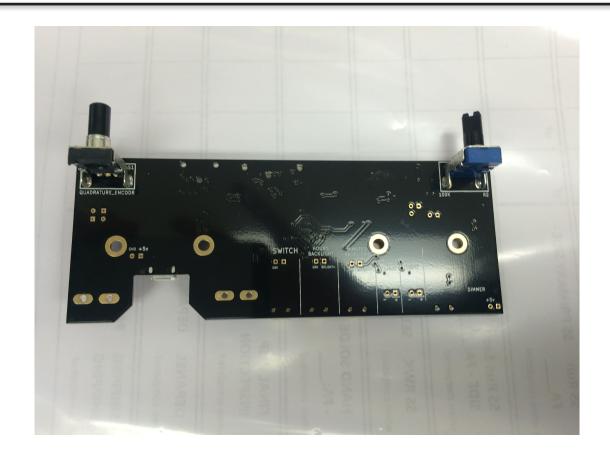






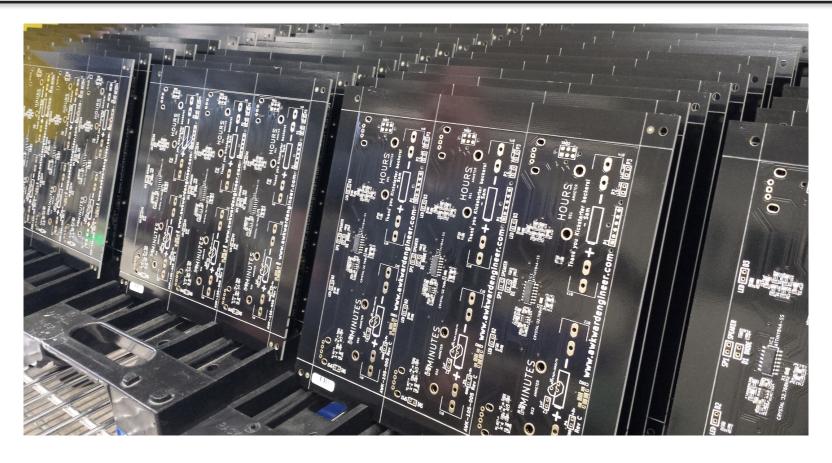






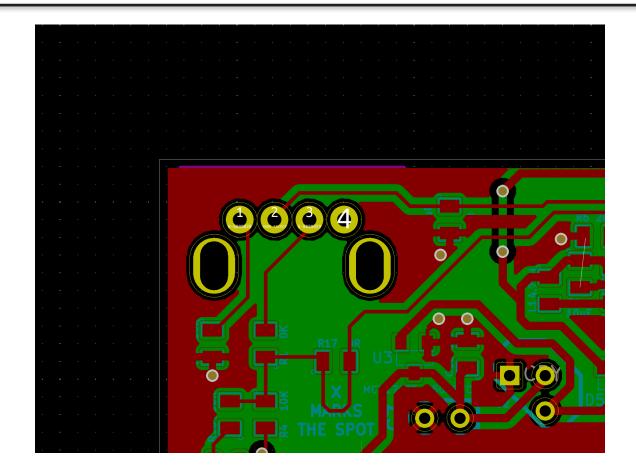






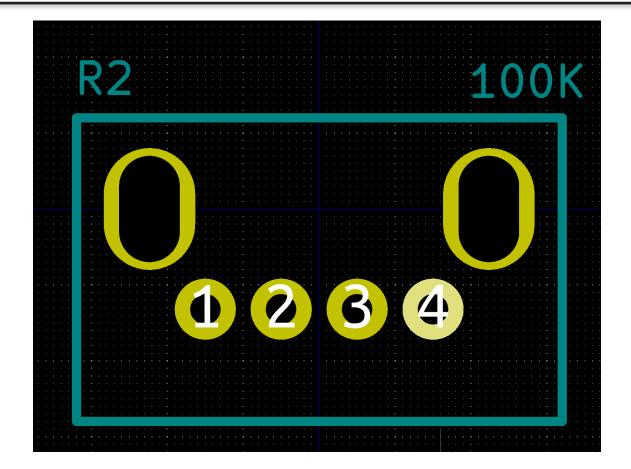








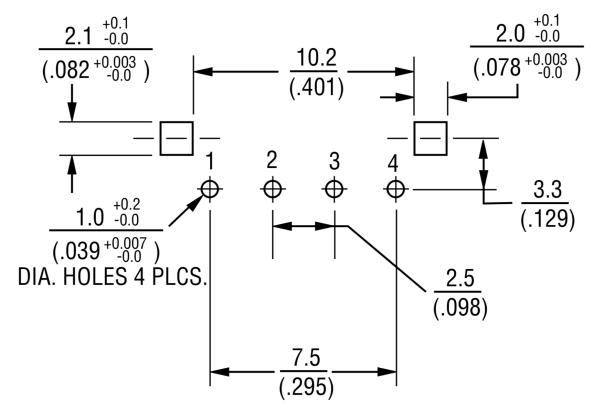






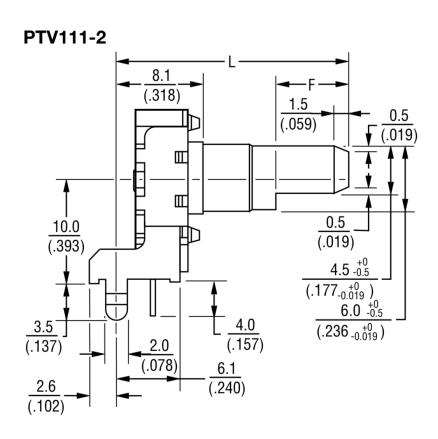






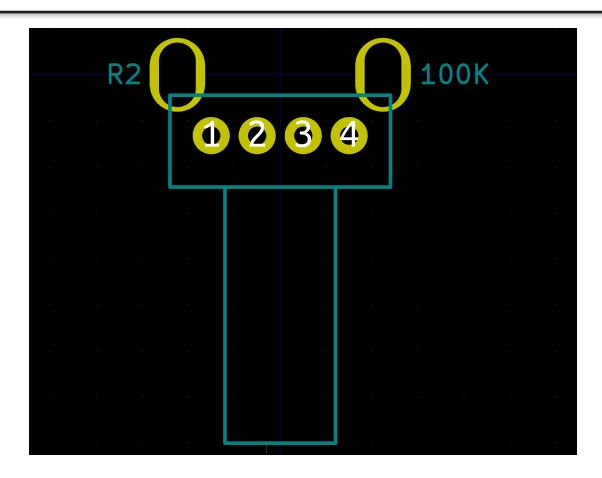






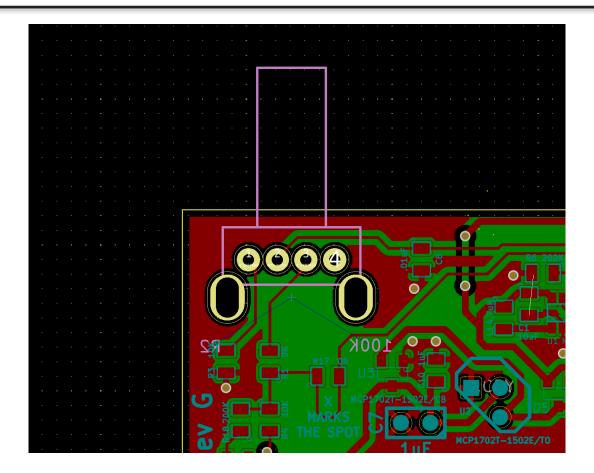






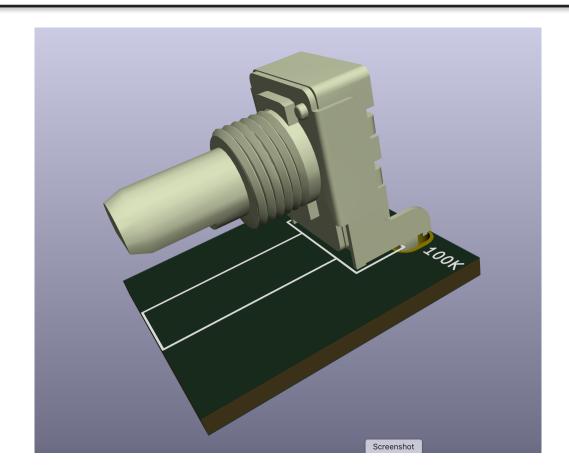






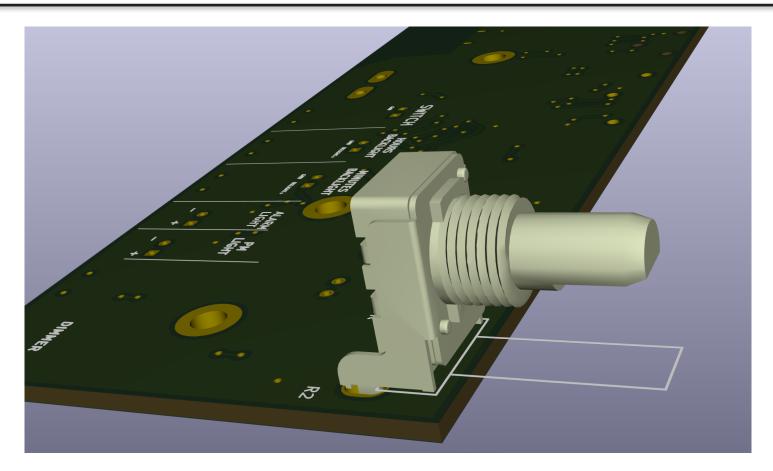














Panelization - Summary



- 1. Add silkscreen representing body of component.
 - 1.1.Doesn't have to be elaborate, just accurate.
 - 1.2.Don't worry, silkscreen that falls outside of the Outline will be trimmed.
- 2. Add 3D Model if you can





- 1. Identifying polarity of components
- 2. Silkscreen legibility
- 3. Panelization
- 4.PCB properties
- 5. Specific manufacturer's part numbers

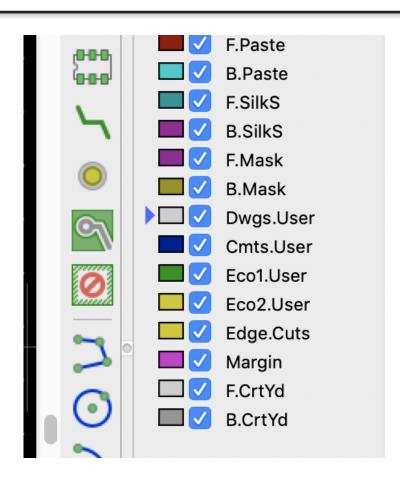




- 1. Number of layers
- 2. Overall PCB thickness
- 3. TG rating
- 4. Inner copper weight
- 5. Outer copper weight
- 6. Silkscreen color
- 7. Soldermask color
- 8. Via-in-pad
- 9. Impedance control
- 10. E-Test Required











		Text Propert	ies	
Text:				
2. PCB Thi 3. TG Ratin 4. Inner Co 5. Outer Co 6. Silkscree 7. Solderm 8. Via-in-P 9. Impedar ohm (+-8%	pper Weight: 0.5oz opper Weight: 1oz en Color: White ask Color: Green ad: Fill and Plate nce Control: Top Layer 2	3.00mil single	e-ended Copla	nar Waveguide 50
Layer:	Dwgs.User ~			
Width:	3	mm	Italic	
Height:	3	mm	Justification:	Left
Thickness:	0.5	mm	Orientation:	0.0
Position X:	25.019	mm	Mirrored	
Position Y:	252.984	mm		
				Cancel OK





• • •	Plot								
Plot format: Gerber	Output directory: Gerber/								
Included Layers	General Options								
✓ F.Cu ✓ B.Cu ✓ F.Adhes ✓ B.Adhes ✓ F.Paste ✓ B.Paste ✓ F.SilkS ✓ B.SilkS	Plot border and title block Plot footprint values Plot footprint references Force plotting of invisible values / refs Exclude PCB edge layer from other layers Exclude pads from silkscreen	Drill marks: Scaling: Plot mode: Default line width: Mirrored plot Negative plot	None	mm					
F.MaskB.MaskDwgs.UserCmts.UserEco1.User	Use auxiliary axis as origin Gerber Options Use Protel filename extensions	✓ Check zone fills Coordinate format:							
✓ Eco2.User ✓ Edge.Cuts ✓ Margin	Generate Gerber job file Subtract soldermask from silkscreen	Use extended X							
Output Messages Plot file "/Users/earldenney/Documents/KiCAD/Clock/Gerber/clock-Eco1_User.gbr" created. Plot file "/Users/earldenney/Documents/KiCAD/Clock/Gerber/clock-Eco2_User.gbr" created. Plot file "/Users/earldenney/Documents/KiCAD/Clock/Gerber/clock-Edge_Cuts.gmt" created. Plot file "/Users/earldenney/Documents/KiCAD/Clock/Gerber/clock-Hargin.gbr" created. Plot file "/Users/earldenney/Documents/KiCAD/Clock/Gerber/clock-Margin.gbr" created. Show: All Frors Warnings Actions Infos									
Run DRC	CI	ose Generate D	Drill Files	lot					





	Plot		
Plot format: PDF	Output directory: Gerber/		
Included Layers	General Options		
F.Mask	✓ Plot border and title block	Drill marks:	None
B.Mask	✓ Plot footprint values	Scaling:	1:1 🗘
✓ Dwgs.User	✓ Plot footprint references	Plot mode:	Filled \$
Cmts.User	Force plotting of invisible values / refs	Default line width:	0.15 mm
Eco1.User Eco2.User	Exclude PCB edge layer from other layers	Mirrored plot	
Edge.Cuts	Exclude pads from silkscreen	Negative plot	
☐ Margin	Do not tent vias		
F.CrtYd	Use auxiliary axis as origin	Check zone fills	before plotting
R.CrtYd			
Output Messages			
Plot file "/Users/earldenney/Docume	nts/KiCAD/Clock/Gerber/clock-F_Paste.gtp" created. nts/KiCAD/Clock/Gerber/clock-F_Paste.gtp" created. nts/KiCAD/Clock/Gerber/clock-B_Paste.gtp" created.		
Plot file "/Users/earldenney/Docume	nts/KiCAD/Clock/Gerber/clock-F_SilkS.gto" created.		
Plot file "/Users/earldenney/Docume	nts/KiCAD/Clock/Gerber/clock-B_SilkS.gbo" created. nts/KiCAD/Clock/Gerber/clock-F_Mask.gts" created.		
	nts/KiCAD/Clock/Gerber/clock-B_Mask.gbs" created.		
Show: All VErrors	S Warnings Actions Infos		Save
Run DRC		Close Generate [Orill Files Plot
Ruii DRC		Juse Generate I	DIIII FIIES PIUL





•				*				'		
	00									
	00			0						
			0	0						
		,	O							
	0 0	0 0	0	0 0						
1. Number of	Lavers: 4									
2 PCR Thicks	ecc. 1 6mm									
 IG Rating: Inner Copp 	TG170 er Weight: 0.5oz									
5. Outer Copp	TG170 er Weight: 0.5oz er Weight: 1oz Color: White							sam@awkwardengineer.com Layout Design: Sam Feller		
7. Soldermasi	k Color: Green							Layout besign: sam retter Schematic Design: Sam Feller Please direct all questions to Sam Feller The Awkward Engineer		
8. Via-in-Pa 9. Impedance	d: Fill and Plate Control: Top Laye	er 23.00mil sind	le-ended Cop	anar Wavequid	e 50 ohm (+-8	3%)		sneet: File: clock.kicad_pcb		
						,	-	Title: Clock Size: A3	Re	Rev: A d: 1/1
								Nicad E.U.A. Ricad (5.1.0-0)	ld.	0: 1/1





- 1. Number of Layers: 4
- 2. PCB Thickness: 1.6mm
- 3. TG Rating: TG170
- 4. Inner Copper Weight: 0.5oz
- 5. Outer Copper Weight: 1oz
- 6. Silkscreen Color: White
- 7. Soldermask Color: Green
- 8. Via-in-Pad: Fill and Plate
- 9. Impedance Control: Top Layer 23.00mil single-ended Coplanar Waveguide 50 ohm (+-8%)





sam@awkwardengineer.com							
Layout Design: Sam Feller							
Schematic Design: Sam Feller							
Please direct all questions to Sam Feller							
The Awkward Engineer							
Sheet:							
File: clock.kicad_pcb							
Title: Clock							
Size: A3 Date: 2019-04-09	Rev: A						
KiCad E.D.A. kicad (5.1.0-0)	ld: 1/1						
7	8						



Define PCB Properties - Summary



- 1. Number of layers
- 2. Overall PCB thickness
- 3. TG rating
- 4. Inner copper weight
- 5. Outer copper weight
- 6. Silkscreen color
- 7. Soldermask color
- 8. Via-in-pad
- 9. Impedance control
- 10. E-Test Required





- 1. Identifying polarity of components
- 2. Silkscreen legibility
- 3. Panelization
- 4. PCB properties
- 5. Specific manufacturer's part numbers





Name	Value	Show	H Align	V Align	Italic	Bold	Text Size
Reference	C7	✓	Left	Center			1.016 mm
Value	1uF	✓	Left	Center			1.016 mm
Footprint	C1	✓	Center	Center			0.762 mm
Datasheet	~	V	Center	Center			1.524 mm
MPN	CL21B105KAFNNNE		Center	Center			1.270 mm
Manufacturer	Samsung		Center	Center			1.270 mm
+ ↑ ↓		Ori	entation		Update F		om Library





Name	Value	Show	H Align	V Align	Italic	Bold	Text Size	
Reference	C7	✓	Left	Center			1.016 mm	
Value	1uF	~	Left	Center		110	1. 16 mm	
Footprint	C1		Center	Cente	115		0.762 mm	
Datasheet	~		Center	(in/er			1.524 mm	
MPN	CL21B105KAFNNNE		C ntur	Center			1.270 mm	
Manufacturer	Samsung	15 0	Center	Center			1.270 mm	
+ ↑ ↓	CL21B105KAFNNNE Samsung	Orio	entation		Update F		om Library	
Library Aufel Unit:	cle: clock-rescue:C Alternate symbol (DeMorgan)		• 0 +90 +180 -90			DefaultMirror around X axisMirror around Y axis		

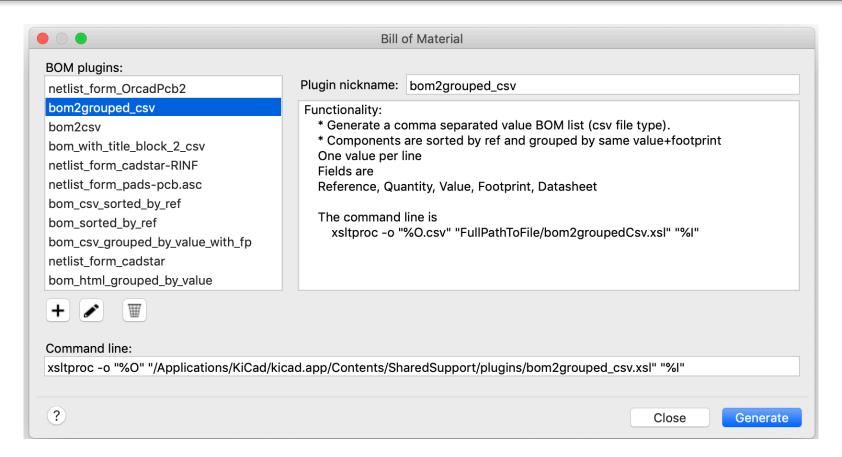




✓ Group symbols	Reference	Value	Footprint	atashe	MPN	Manufacturer	Qty
	R17	0R	SM0805	~	DNP		1
Field Show Group By	> R1, R16	OK	SM0805	~	ERJ-6GEY0R00V	Panasonic	2
Reference	> C2, C4	12.5pF	SM0805	~	CL21C120JB61PNC	Samsung	2
Footprint	> C5, C6, C8	.01uF	SM0805	~	CL21B103KBANNNC	Samsung	3
Datasheet	C7	1uF	C1	~	CL21B105KAFNNNE	Samsung	1
MPN 🔽	C10	1uF	SM0805	~	CL21B105KAFNNNE	Samsung	1
Manufacturer	L1	4.7uH	SM0805	~	LQM21NN4R7K10L	Murata	1
	> C1, C3	10uF	SM0805	~	CL21B106KOQNNNE	Samsung	2
	> R13-R15	220	SM0805	~	ERJ-6GEYJ221V	Panasonic	3
	> R3, R4, R9, R12	10K	SM0805	~	RMCF0805FT10K0	Stackpole	4
	> R7, R8	33K	SM0805	~	ERJ-6ENF3302V	Panasonic	2
	> R10, R11	51K	SM0805	~	ERJ-6GEYJ513V	Panasonic	2
	R2	100K	Chris_Denney_Library:bourns_knob	~	PTV111	Bourns	1
	R5	130K	SM0805	~	ERJ-6ENF1303V	Panasonic	1
	> R6, R18	200K	SM0805	~	ERJ-6ENF2003V	Panasonic	2
	> DS1, DS2	AMMETER	ammeter		DNP		2
	IC1	ATTINY84A-SS	SO14E		ATTINY84A-SSU	Microchip	1
	CON1	AVR-ISP-6	ISPheader		DNP		1
	> BT1, BT2	BATTERY_CLIP	AA_Battery_Clip_THRU_HOLE_BK-92		92	Keystone	2
Add Field	> P2-P4, P8, P10	CONN_2	SIL-2		DNP		5

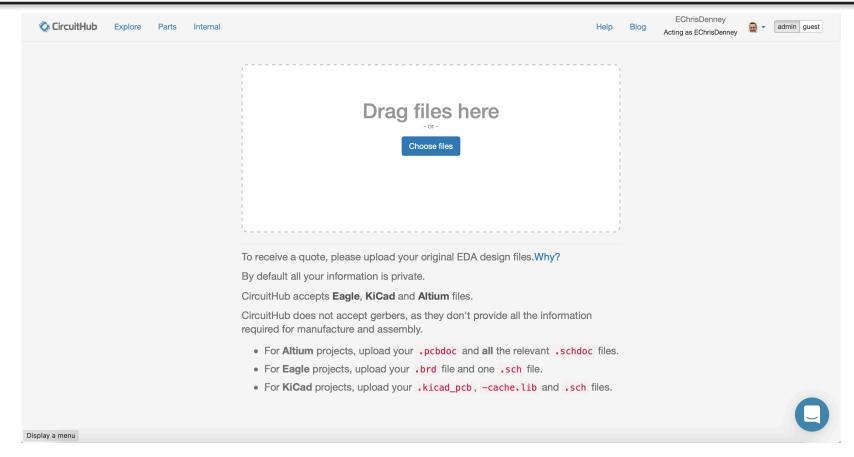






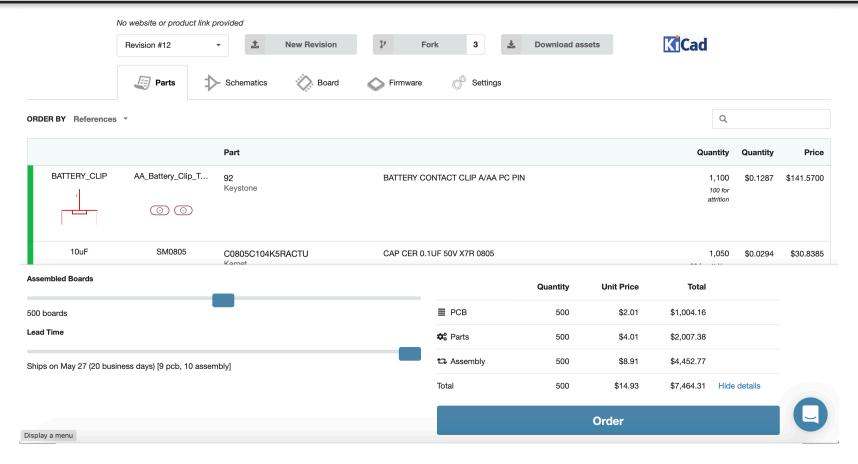






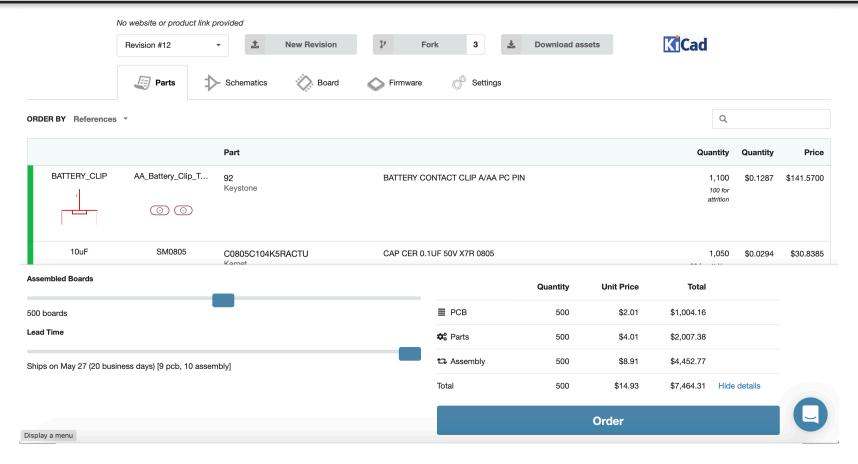
















Assembled Boards

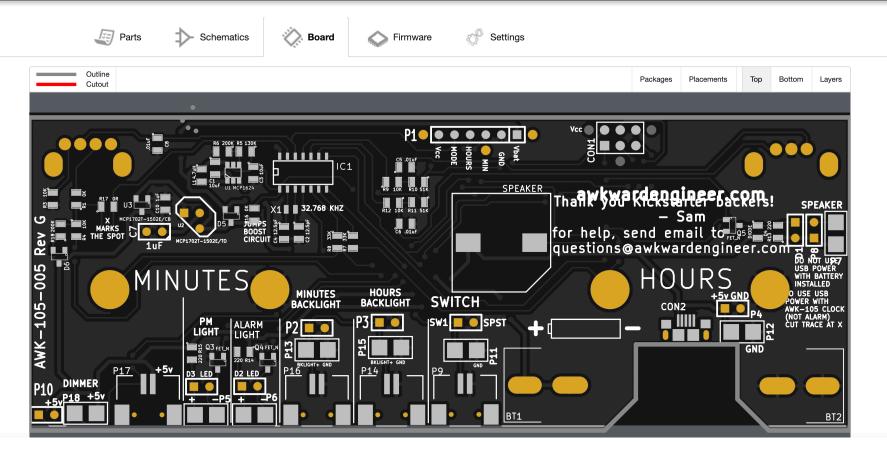
500 boards

Lead Time

Ships on May 27 (20 business days) [9 pcb, 10 assembly]











Color	Stackup					
Soldermask color	Silkscreen color		Board thickness (1)			
Black	White	₩	1.6			*
		☑ Edit	Copper weight			
Missellanseus			Outer 1	Inner	Not specified ▼	
Miscellaneous						
Cutouts			- O FD4 TO 400 405	O ED4111 1 -		
Board does not contain cutouts		~	Material 1 FR4 TG 130-135	FR4 High	IG	
Via fill			Custom stackup (1)			
No via fill required			Add custom stackup			
Add via fill locations			Add Custom Stackup			
Via in pad 🐧						☑ Edit
No via in pad fill required						
Add locations which require filling	and plating		Specifications			
Castellated edges			•			
Does not require castellated edges		~	Width		133.35	mm
Blind/Buried layer sets 1			Length		50.81	mm
0			Number of layers		2	



Specific MPN - Summary



- 1. Include Manufacturer
- 2. Include MPN
- 3. Do this when you assign footprint
- 4. Real legitimate quotes in seconds not days using CircuitHub







- 1. Identifying polarity of components
- 2. Silkscreen legibility
- 3.Panelization
- 4.PCB properties
- 5. Specific manufacturer's part numbers





- 1. Use square pads or clear silkscreen.
- 2.1x1mm character size. 0.18mm lines.
- 3. Draw overhanging parts
- 4.Include PCB properties in dwgs.User
- 5.Add Manufacturer and MPN to symbols





Bonus Tip



Center Pad of QFN/QFP



Gen	eral Local Clearance	and Settings	Custom Shape Primitives		Footprint REF** (LFCSP-16-1EP_3x3mm_P0.5mm_EP1.6x1.6mm),
Pad number:	17		Hole shape: Circular	\$	front side, rotated 0.0 deg
Net name:	<no net=""></no>	~	Hole size X: 0	mm	
Pad type:	SMD	\$	Hole size Y: 0	mm	
Shape:	Rounded Rectangle	©	0		
Position X:	0	mm	Copper: F.Cu	\$	
Position Y:	0	mm	Technical layers: F.Adhes		
Size X:	1.6	mn	B.Adhes		
Size Y:	1.6	mm ⁴	F.Paste		
Orientation:	0.0	v deg	B.Paste F.SilkS		
Shape offset X:	0	mm	B.SilkS		
Shape offset Y:	0	mm	✓ F.Mask		
Pad to die length:	0	mm	B.Mask Dwgs.User		
Trapezoid delta:	0	mm	Eco1.User		
Trapezoid axis:	Vertical	\$	Eco2.User		_
Corner size:	15.6	%			Show pad in outline mode
Corner radius:	0.2496	mm			



Center Pad of QFN/QFP



Ger	neral	Local Clearance and Se	ttings	Custom Shap	e Primitives		Footprint REF** (LFCSP-16-1EP_3x3mm_P0.5mm_EP1.6x1.6mm),
Pad number:	17			Hole shape:	Circular	\$	front side, rotated 0.0 deg
Net name:	<no< th=""><th>net></th><th></th><th>Hole size X:</th><th>0</th><th>mm</th><th></th></no<>	net>		Hole size X:	0	mm	
Pad type:	SME)		Hole size Y:	0	mm	
Shape:	Roui	nded Rectangle		0	F.O.,	\$	
Position X:	0		mm		F.Cu	<u> </u>	
Position Y:	0		mm	Technical I			
Size X:	1.6		mn	B.Adhe			
Size Y:	1.6		mm	✓ F.Paste			
Orientation:	0.0		deg	B.Paste F.SilkS			
Shape offset X:	0		mm	B.SilkS			
Shape offset Y:	0		mm	✓ F.Mask			
Pad to die length	0		mm	B.Mask Dwgs.U			
Trapezoid delta:	0		mm	Eco1.Us	ser		
Trapezoid axis:	Vert	ical 🗘		Eco2.U	ser		
Corner size:	15.6		%				Show pad in outline mode
Corner radius:	0.249	96	mm				



Topics Cut From Presentation



- Gang soldermask problems
- Plated hole sizes
- Fiducials
- Smallest component sizes
- Single sided vs double sided
- SMT parts being too close to thru-hole
- Cutouts
- Wrong footprints or part numbers
- Your 0402 footprint is probably awful
- Solder paste 1:1 with copper
- Overhanging microUSB ports
- Paste on hybrid components (SMT and Thru-hole in one part)







More Info worthingtonassembly.com/best-practices

echrisdenney.com



Thank you!



Chris Denney - CTO - Worthington Assembly Inc.
Chris Denney - Jerk That Tells You There's a Problem - CircuitHub Inc.

cdenney@worthingtonassembly.com @WAssembly on Twitter

Thank to Sam Feller (aka The Awkward Engineer) for letting me use his project in this presentation https://www.awkwardengineer.com/